Defense Microelectronics Activity (DMEA)
22.1 Small Business Innovation Research (SBIR)
Proposal Submission Instructions

INTRODUCTION

The Defense Microelectronics Activity (DMEA) SBIR/STTR Program is implemented, administrated, and managed by the DMEA Office of Small Business Programs (OSBP). Proposers responding to a topic in this BAA must follow all general instructions provided in the Department of Defense (DoD) SBIR Program BAA. DMEA requirements in addition to or deviating from the DoD Program BAA are provided in the instructions below.

Specific questions pertaining to the administration of the DMEA SBIR/STTR Program and these proposal preparation instructions should be directed to the DMEA SBIR/STTR Program Manager (PM), Mr. Greg Davis, at osd.mcclellan-park.dmea.list.smbus@mail.mil.

PHASE I PROPOSAL GUIDELINES

The Defense SBIR/STTR Innovation Portal (DSIP) is the official portal for DoD SBIR/STTR proposal submission. Proposers are required to submit proposals via DSIP; proposals submitted by any other means will be disregarded. Detailed instructions regarding registration and proposal submission via DSIP are provided in the DoD SBIR Program BAA.

DMEA intends for Phase I to be only an examination of the merit of the concept or technology that still involves technical risk, with a cost not exceeding $167,500 (excludes Discretionary Technical and Business Assistance (TABA) amount). The technical period of performance for the Phase I effort should be no more than six (6) months.

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA's core research and development requirements.

Please ensure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, e-mail address, or company official after proposal submission.

PROPOSAL VOLUMES:

Proposal Cover Sheet (Volume 1)

Required per the DOD SBIR Program BAA.

Technical Volume (Volume 2)

The technical volume is not to exceed 20 pages and must follow the formatting requirements provided in the DoD SBIR Program BAA.

Content of the Technical Volume

Read the DOD SBIR Program BAA for detailed instructions on proposal format and program requirements. When you prepare your proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be entertained.

DMEA will evaluate and select Phase I proposals using the evaluation criteria contained in Section 6.0 of the DOD SBIR Program BAA . Due to limited funding, DMEA reserves the right to limit awards under any topic, and only proposals considered to be of superior quality will be funded.

Cost Volume (Volume 3)

DMEA does not accept Phase I proposals exceeding $167,500. DMEA will conduct a price analysis to determine whether cost proposals, including quantities and prices, are fair and reasonable. Contractors should expect that cost proposals will be negotiated. Costs must be separated and clearly identified on the Proposal Cover Sheet (Volume 1) and in Volume 3.

The on-line cost volume for Phase I and Phase II proposal submissions must be at a level of detail that would enable DMEA personnel to determine the purpose, necessity, and reasonability of each cost element. Provide sufficient information (a. through h. below) on how funds will be used if the contract is awarded. Include the itemized cost volume information (a. through h. below) as an appendix in your technical proposal. The itemized cost volume information (a. through h. below) will not count against the 20-page limit on Phase I and II proposal submissions.

a. Special Tooling and Test Equipment and Material: The inclusion of equipment and materials will be carefully reviewed relative to need and appropriateness of the work proposed. The purchase of special tooling and test equipment must, in the opinion of the Contracting Officer, be advantageous to the government and relate directly to the specific effort. They may include such items as innovative instrumentation and/or automatic test equipment. Title to property furnished by the Government or acquired with Government funds will be vested with the DOD Component; unless it is determined that transfer of the title to the contractor would be more cost effective than recovery of the equipment by the DOD Component.

b. Direct Cost Materials: Justify costs for materials, parts, and supplies with an itemized list containing types, quantities, price, and where appropriate, purposes.

c. Other Direct Costs: This category of costs includes specialized services such as machining or milling, special testing or analysis, costs incurred in obtaining temporary use of specialized equipment. Proposals, which include teased hardware, must provide an adequate lease *versus* purchase justification or rationale.

d. Direct Labor: Identify key personnel by name if possible or by labor category if specific names are not available. The number of hours, labor overhead and/or fringe benefits and actual hourly rates for each individual are also necessary.

e. Travel: Travel costs must relate to the needs of the project. Break out travel cost by trip, with the number of travelers, airfare, and per diem. Indicate the destination, duration, and purpose of each trip.

f. Cost Sharing: Cost sharing is permitted. However, cost sharing is not required, nor will it be an evaluation factor in the consideration of a proposal.

g. Subcontracts: Involvement of university or other consultants in the planning and /or research stages of the project may be appropriate. If the offeror intends such involvement, describe the involvement in detail and include information in the cost proposal. The proposed total of all consultant fees, facility leases, or usage fees and other subcontract or purchase agreements may not exceed one-third of the total contract price or cost, unless otherwise approved in writing by

the Contracting Officer. Support subcontract costs with copies of the subcontract agreements. The supporting agreement documents must adequately describe the work to be performed (i.e., Cost Volume). At the very least, a statement of work with a corresponding detailed cost volume for each planned subcontract must be provided.

h. Consultants: Provide a separate agreement letter for each consultant. The letter should briefly state what service or assistance will be provided, the number of hours required, and the hourly rate.

Company Commercialization Report (CCR) (Volume 4)
Completion of the CCR as Volume 4 of the proposal submission in DSIP is required. Please refer to the DoD SBIR Program BAA for full details on this requirement. Information contained in the CCR will be considered by DMEA during proposal evaluations.

Supporting Documents (Volume 5)
Other than the Volume 5 requirements listed in the DoD SBIR Program BAA, supporting documents are not required and will not be evaluated.

Fraud, Waste and Abuse Training (Volume 6)
Fraud, Waste and Abuse (FWA) training is required for Phase I and Direct to Phase II proposals. Please refer to the DoD SBIR Program BAA for full details.

PHASE II PROPOSAL GUIDELINES
Phase II proposals may only be submitted by Phase I awardees. Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. DMEA encourages, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II efforts.

Phase II proposals may be submitted for an amount not to exceed $1,100,000. The technical period of performance for the Phase
II effort should be no more than twenty-four (24) months.

Phase I awardees may submit a Phase II proposal without invitation not later than sixty (60) calendar days following the end of the Phase I contract. The Phase II proposal submission instructions are identified in the Phase I contract, Part I – The Schedule, Section H, Special contract requirements, “SBIR Phase II Proposal Submission Instructions.”

All Phase II proposals must have a complete electronic submission per the Proposal Volumes area listed in Phase I. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or it will not be considered for award.

Due to limited funding, DMEA’s ability to award any Phase II, regardless of proposal quality or merit, is subject to availability of funds. Please ensure that your proposal is valid for 120 days after submission, and any extension to that time period will be requested by the contracting officer.

Any follow-on Phase II proposal (i.e., a second Phase II subsequent to the initial Phase II effort) shall be initiated by the Government Technical Point of Contact for the initial Phase II effort and must be approved by the DMEA SBIR/STTR Program Manager in advance.

DMEA SBIR PHASE II ENHANCEMENT PROGRAM
To encourage transition of SBIR into DOD systems, DMEA has a Phase II Enhancement policy. DMEA’s Phase II Enhancement program requirements include: up to one-year extension of existing Phase II, and

up to $550,000 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase II Enhancement funds by modifying the Phase II contract.

DISCRETIONARY TECHNICAL AND BUSINESS ASSISTANCE (TABA)
DMEA does not provide Discretionary Technical and Business Assistance (TABA).

EVALUATION AND SELECTION
All proposals will be evaluated in accordance with the evaluation criteria listed in the DoD SBIR Program BAA. Proposing firms will be notified of selection or non-selection status for a Phase I or Phase II award within 90 days of the closing date of the BAA.

Refer to the DoD SBIR Program BAA for procedures to protest the Announcement. As further prescribed in FAR 33.106(b), FAR 52.233-3, Protests after Award should be submitted to:

DMEA SBIR/STTR Program Manager (PM):

- Name: Mr. Greg Davis
- Email: osd.mcclellan-park.dmea.list.smbus@mail.mil

DMEA SBIR Phase I Topic Index

DMEA221-001 Synthesizable Register Transfer Logic (RTL) Assertions

DMEA221-001 TITLE: Synthesizable Register Transfer Logic (RTL) Assertions

OUSD (R&E) MODERNIZATION PRIORITY: Microelectronics

TECHNOLOGY AREA(S): Electronics

OBJECTIVE: Develop a library of practical synthesizable register transfer logic (RTL) assertions (System Verilog is highly preferred), investigate limitations of synthesizable assertions in both integrated circuit (IC) and field programmable gate array (FPGA) design and design verification flows using already existing EDA platforms, and develop a methodology for synthesizable RTL assertions and error reporting. Identify robust test vehicles and implement synthesizable RTL assertions in both an FPGA and an IC.

DESCRIPTION: In the design verification (DV) of digital circuit design, it is very common for the RTL coder to include assertions in their RTL code, commonly known as assertion-based verification (ABV). These assertions are non-synthesizable as their purpose is solely for design verification, and add nothing to the mission mode of the RTL. They are used in the design verification process to monitor that correct signals, timing and sequences are being maintained. However, for hardware assurance, it may be desirable in the mission mode to have additional circuitry that monitors that correct signals, synchronous timing and sequences are being maintained. Some prior research has been done and involve the creation of a novel synthesis compiler [1], or requiring the use of high level synthesis (HLS) compilers [2]. However, most digital designers will not have access to customer compilers or HLS compilers. And some prior research has been done [3-5] but not fully realized with practical digital design and digital design verification (DV) best practices for FPGA and digital IC development.

PHASE I: Perform a feasibility study that defines a commonly used IC electronic design application (EDA) platform, and a commonly used FPGA design platform for the investigation. The investigation will not involve creating a new synthesis tool or compiler, but to use industry standard EDA tools. Investigate and develop appropriate test vehicles, either organic or procured. Many practical assertions involve comparing signals at different RTL hierarchy modules. But for more efficient area, many times hierarchies are flattened during synthesis. Also, it would be desirable to be to have some assertions to be synthesized and some not. Investigate the practicality and any limitations of synthesizable RTL assertion code (System Verilog is highly preferred, research has already been done on synthesizable ANSI-C assertions [2]) in both IC and FPGA platforms regarding best practices in digital design and digital DV including (but not limited to): lint, clock domain crossing (CDC), reset domain crossing (RDC), synthesis design constraints (SDC), signal hierarchy, synthesis, scan chain insertion, area, logic equivalence check (LEC) and code coverage. Additionally, propose a practical methodology for how synthesizable assertions and error reporting are integrated into the digital design flow for both IC and FPGA development.

PHASE II: Phase II will result in building, testing and delivering a fully functional prototype or technology of the method developed in phase I. Identify robust test vehicles. Review lint, clock domain crossing (CDC) and reset domain crossing (RDC) reports. Review synthesis design constraints (SDC) file. Perform thorough design verification (DV) including (but not limited to): a functional verification matrix (FVM), a means of monitoring the progress and completion of the FVM, unified top-level test bench, definition of constrained random variables (CRV's), proper regression runs based on the state space of the CRV's, and code coverage reports. RTL code should have assertions, with some assertions monitoring signals at different levels of code hierarchy. Assertions need to be tested against false positives and false negatives. For the IC platform, review synthesis scripts. Perform synthesis with no assertions synthesized, and some chosen assertions synthesized in both IC and FPGA platforms with the hierarchy flattened. For the IC platform, insert a scan chain and enable clock gating during synthesis. For

the FPGA platform, continue through implementation phase (with and without synthesized assertions), and prove functionality of the FPGA. For the IC platform, review place and route scripts, review place and route reports, static timing analysis reports, LEC reports and perform automated test pattern generation (ATPG). Actual manufacturing of the IC would be ideal, but may not be practical.

PHASE III DUAL USE APPLICATIONS: Phase III will result in error monitoring that would be useful in commercial applications as part of built-in self-test BIST, having potential benefits of improved performance robustness and test time savings. During a Phase III program, offerors may refine the performance of the design and produce pre-production quantities for evaluation by the Government.

REFERENCES:

1. Y. Oddos, et al, "From Assertion-based Verification to Assertion-based Synthesis", 17th International Conference on Very Large Scale Integration, Oct 2009.
2. Mohamed Hammouda, et al, "A Design Approach to Automatically Synthesize ANSI-C Assertion During High-Level Synthesis of Hardware Accelerators" 2014 IEEE International Symposium on Circuits and Systems, June 2014.
3. Ivan Kastelan, Zoran Krajacevic, "Synthesizable SystemVerilog Assertions as a Methodology for SoC Verification", First IEEE Eastern European Conference of Computer Based Systems, 2009.
4. Sayantan Das, et al, "Synthesis of System Verilog Assertions" EDAA, 2006.
5. Omar Amin, et al, "System Verilog Assertions Synthesis Based Compiller" 17th International Workshop on Microprocessors and SOC Test and Verification", 2016.

KEYWORDS: FPGA; Digital ASIC; Design Verification; Hardware Assurance

TPOC-1: Paul Wong
Phone: (916) 999-2683
Email: paul.wong14.civ@mail.mil